

IN THE CLAIMS:

Please amend claims 22, 31, 32 and 42 as set out in the following listing of the claims:

1-21 (Cancelled).

22. (Currently Amended) A method for modifying a processing sequence for implementation and control of a processing apparatus by editing the configuration of a processing web, comprising the steps of:

determining a current state of said processing web; and

editing at least one processing element of said processing web;

whereby said processing sequence for implementation and control of said processing apparatus is modified in accordance with the editing of said at least one processing element.

23. (Original) The method of claim 22, further comprising the step of updating said first processing element indicating a time during which said first processing element is to consume additional input data.

24. (Original) The method of claim 23, wherein said update is controlled by an update processing element.

25. (Original) The method of claim 22, wherein said editing of said at least one processing element includes changing a connection of at least one pin of said at least one processing element.

26. (Original) The method of claim 22, wherein said editing of said at least one processing element includes adding another processing element to said processing web.

27. (Original) The method of claim 26, wherein said another processing element is added to said processing web by dragging a representation of said processing element onto a display representative of said processing web, and connecting inputs and outputs of said another processing element to the inputs and outputs of other existing processing elements.

28. (Original) The method of claim 22, wherein said editing of said at least one processing element includes modifying the definition thereof.

29. (Original) The method of claim 28, wherein modifying the definition of said at least one processing element includes modifying one or more operating parameters thereof.

30. (Original) The method of claim 22, further comprising the step of adding a viewing element to said graphical representation of said processing web to view a live, real time output at the location of said viewing element.

31. (Currently Amended) A method for modifying a processing sequence for implementation and control of a processing apparatus by editing the graphical representation of a processing web as displayed on a processing web editor, comprising the steps of:

determining a current state of said processing web for implementation and control of said processing apparatus;

generating a graphical representation of said processing web for implementation and control of said processing apparatus by:

determining a first processing element of said processing web;

placing said first processing element in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

determining a second processing element of said processing web;

placing said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

connecting at least one pin of said first processing element to one pin of said second processing element; and

editing at least one processing element of said processing web;

whereby said processing sequence for implementation and control of said processing apparatus is modified in accordance with the editing of said at least one processing element.

32. (Currently Amended) A graphical representation of a processing web ~~of an instrument, for implementation and control of a processing apparatus~~ comprising:

a first processing element of said processing web, said first processing element being placed in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

a second processing element of said processing web, said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

a connection for connecting at least one pin of said first processing element to one pin of said second processing element.

33. (Original) The graphical representation of the processing web of claim 32, wherein said connection connects an output pin of said first element to an input pin of said second element.

34. (Original) The graphical representation of the processing web of claim 33, wherein said connection generates a line in said graphical representation between said output pin of said first element to said output pin of said second element.

35. (Original) The graphical representation of the processing web of claim 33, wherein said line is drawn including one of a plurality of designations based upon a type of data being carried thereon.

36. (Original) The graphical representation of the processing web of claim 35, wherein said plurality of designations are colors.

37. (Original) The graphical representation of the processing web of claim 32, wherein said at least one pin of said first processing element and said at least one pin of said second processing element are coded based upon a type of data to output therefrom, or received thereby, respectively.

38. (Original) The graphical representation of the processing web of claim 37, wherein said coding is by color.

39. (Original) The graphical representation of the processing web of claim 37, wherein said coding is by symbol

40. (Original) The graphical representation of the processing web of claim 37, wherein said coding is by graphical designation.

41. (Original) The graphical representation of the processing web of claim 32, wherein said first processing element is updated at a faster rate and said second processing element is updated at a slower rate.

42. (Currently Amended) The graphical representation of the processing web of claim

41, wherein said update of said first processing element and update of said second processing element are synchronized.

43. (Original) The graphical representation of the processing web of claim 41, wherein said update of said first and second processors is controlled by an update processing element.

44. (Original) The graphical representation of the processing web of claim 32, wherein a viewing object may be placed at any location on the graphical representation to see a current, live output at that location.

45-77 (Cancelled).